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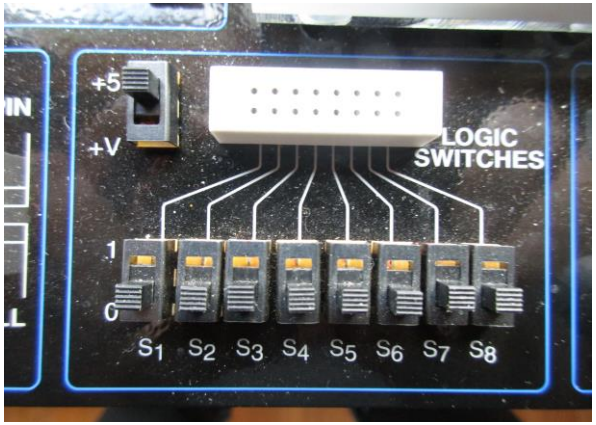
Lab 11

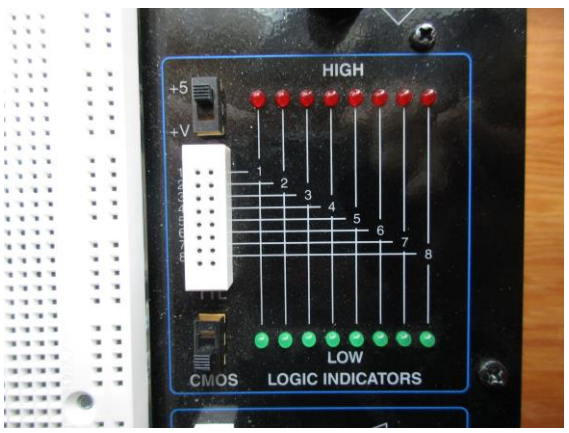
This lab will investigate the "truth tables" of several varieties of digital integrated circuits. For this lab we will be using the trainer with the 5 volt power supply.

The devices we will be using are "CMOS" (Complementary Metal Oxide Semiconductor) integrated circuits. While CMOS will work quite well from supply voltages from +3 to +15 volts (and some will go as high as +20 volts) for us to be compatible with some other types of digital ICS, we will stick with the common +5 volt supply.

TRAINER SWITCHES AND INDICATORS



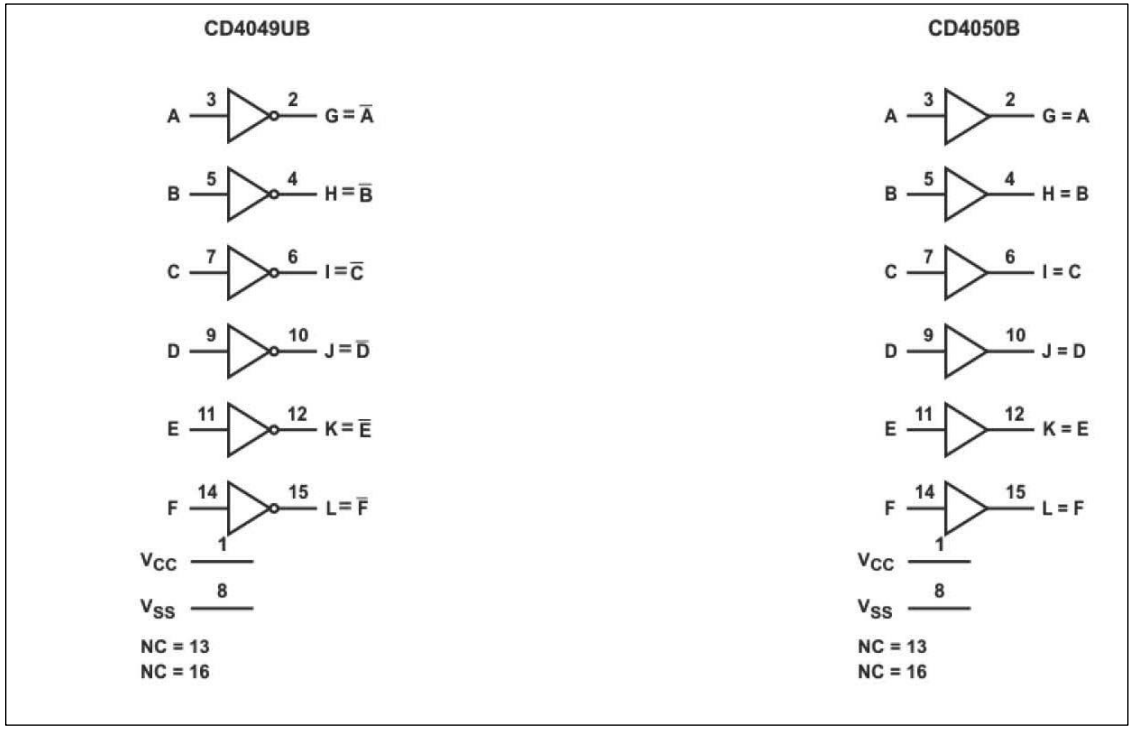
The 8 switches in the lower left corner of the trainer may be set to go to the V+ supply set at the top yellow terminal of the trainer or they can be common-switched to the +5 supply as well. Please set the switch to the +5 volt position. Note that the 8 switches will provide a digital low (0) or a digital high (1) depending on the position of the individual switches.



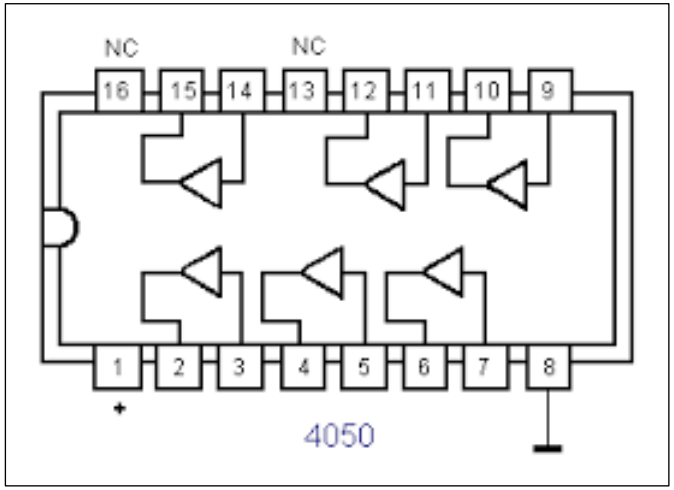
In the upper right corner of the trainer there are 8 logic indicators, and again we have the choice as to whether to reference digital high and low to the +V or +5 volt supply. Reference the indicators to the +5 supply.

1. Connect switch S1 to Logic Indicator #1. Switch S1 between low and high and note that the appropriate indicator lights.
2. Test switches S2-S8 individually to prove that they all work.
3. Use any switch (now that we know that they all work correctly) and test logic indicators 2-8 to prove that they all work.

4050 Hex (6 position) BUFFER
4049 Hex INVERTING BUFFER

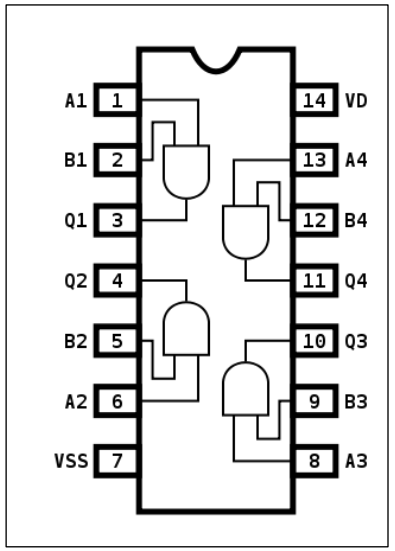


1. For all CMOS devices, VCC means connect this pin to the logic high power supply (+5 volts) and Vss means connect this pin to the logic low (ground) point.
2. NC means that this pin should not have a connection. For most devices this simply means that the pin has no connection whatsoever, but for some devices it is connected internally and you may destroy the device by connecting it.
3. For all CMOS devices, any unused input must be tied SOMEWHERE, either high or low. Inputs for the buffers are letters A through F.
4. For the 4050 Hex Buffer, connect pin 3 (A) to any one of the switches 1-8 in the lower left corner of the trainer (see pinout diagrams to the right). If we follow paragraph (3) above, then pins B through F should either go to +5 or to ground (your choice).
5. Connect pin 2 (G) to Logic Indicator #1. Does a high on the input produce a high on the indicator? Does a low on the input produce a low on the output?
6. If we wanted to really test the entire IC, then we would repeat (4) and (5) above on each of the individual buffers B through F, although that would take a fair amount of time and is not really necessary at this time.



7. Repeat steps (4) through (6) for the 4049 INVERTING buffer and note that the Logic indicators should show that for a HIGH on the input you get a LOW on the output.

4081 AND Gate
4011 NAND Gate



The two images to the right may be confusing at first until you understand that rarely do two sources call the same pins the same thing. The artist that did the top view of the package called the inputs A and B and the output Q. The artist that drew the truth table (below) called the inputs X and Y and the output Z (which is by far the more common way of doing it).

Note that there are four separate gates in the package, and the drawing depicts 4081 AND gates. We will figure out how to translate this into the 4011 NAND gate quite easily.

1. Connect the two inputs of any one gate (for example, A1 and B1) to separate switches (for example S1 and S2) and switch them both high (1) and the output (Q1) to a Logic indicator.

   (Don't forget you have to connect Vdd (pin 14) to the +5 supply and the Vss (pin 7) to ground for the IC to work.)

2. The output indicator should show a HIGH level for both S1 and S2 high (1).
3. Switching either S1 or S2 low (0) should cause the indicator to show low.
4. Switching both S1 and S2 should also show the indicator to show low.

5. Converting this AND gate to the 4011 NAND gate is quite easy. For ONLY the outputs, what was high is now low and what was low is now high. For example, if both NAND inputs are high, the output is low. If either input (or both) is low, the output will be high.

6. Repeat the steps (1) through (4) for a 4011 NAND gate.

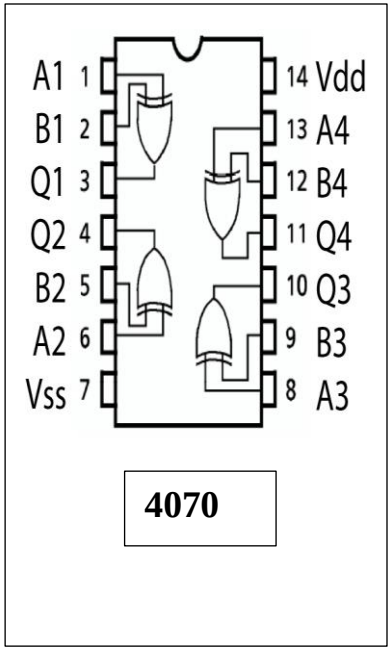
Inputs		Outputs
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

4071 OR Gate
4001 NOR Gate
4070 XOR (Exclusive OR gate)

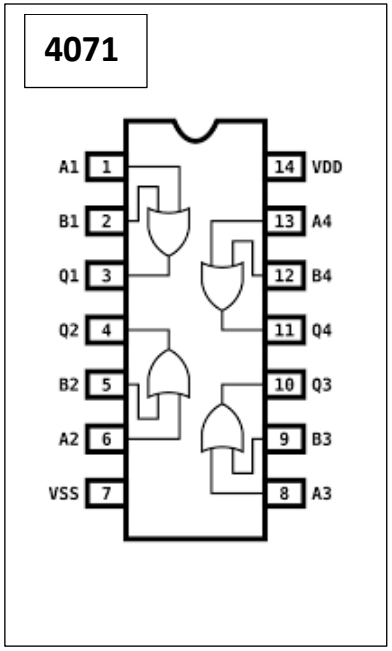
The basic OR gate says that it doesn't matter which input is high, the output will be high. The only case in which the output is low is if BOTH inputs are low.

Unfortunately the stockroom doesn't have any 4071 OR gates, but see if you can figure out how to make an OR gate out of a NOR gate and a 4049 inverting buffer.

Now we come to a more complex gate, the 4070 Exclusive OR gate. The XOR says that EITHER A ** OR ** B can be high for a high output, but if BOTH are high, the output is low. Prove that this is true using switches and logic indicators, and draw the truth table below the 4071 OR gate table.



4070



INPUT		OUTPUT
A	B	C=A+B
0	0	0
0	1	1
1	0	1
1	1	1

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********** End of Lab 11**********